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EXAMINER	
WOLVERTON, DAREN A	
ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,483	HAGEN ET AL.	
	Examiner	Art Unit	
	DAREN WOLVERTON	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30-33* is/are allowed.

6)☒ Claim(s) *15-18,20-25,27-29 and 34* is/are rejected.

7)☒ Claim(s) *19 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the semiconductor chip of the base semiconductor component electrically connected to the contact pads via bonding wire connections, wherein the semiconductor chip faces toward the wiring substrate (claim 23) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Regarding claim 23, the claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Notably the applicant fails to disclose how the chip may be mounted with the active side facing the substrate (as required by the amended claim 15) but still be wire bonded to contact pads on the upper side of the wiring substrate. The applicant does disclose the use of wire bonds in paragraph [0053] (of the PGPUB), but that paragraph seems to simply disclose the use of a normal active side up form of the wire bonding chips as an alternative to flip chip bonding (evidenced by the requirement to use plastic composition 27 to encapsulate the wire bonds) and thus fails to convey the possession of the claimed invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15, 18, 20, 29, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 7,006,360) (Kim hereinafter).

Regarding claim 15, Kim discloses, in FIG. 6A, FIG. 6C, and FIG. 8, a base semiconductor component for a semiconductor component stack comprising: a semiconductor chip 604 arranged on a stiff wiring substrate 602 (called a printed circuit board by Kim), wherein an active upper side (the side with the solder balls 610) of the semiconductor chip 604 faces towards the wiring substrate 602 (shown in FIG. 6A), the wiring substrate 602 having contact pads 614 on its upper side in edge regions (shown in FIG. 6A) and external contacts 616 (called solder balls by Kim, and shown in FIG. 6C) of the base semiconductor component on its underside opposite to the semiconductor chip 602; contact areas (the solder balls 610 in FIG. 6A) of an integrated circuit of the active upper side of the semiconductor chip 604, the external contacts 616, and the contact pads 614 are electrically connected (see column 4, lines 25-29 and column 6, lines 58-62) to one another via wiring lines (as the wiring substrate is a printed circuit board) and through contacts (not explicitly disclosed by Kim but shown in FIG. 1 and FIG. 2 and thus implied as present in the invention of Kim) of the wiring substrate 602; a deformable interconnection film 608/800 (see FIG. 6A, FIG. 8, and

column 6, lines 53-65, and note that the alternate embodiment using TAB tape is being used in this rejection and the tape is deformable) defines an upper side of the base semiconductor component and has a freely accessible arrangement pattern of stack contact areas (shown as circles in FIG. 8) arranged congruently with respect to external contacts of a semiconductor component 606 to be stacked; the interconnection film 608/800 is deformed (shown in FIG. 6A, note that as this is a product claim, deforming is read as [bent towards] not [formed by deformation]) in its edge regions toward the contact pads 614 of the wiring substrate 602; and the stack contact areas are electrically connected (see FIG. 8 and column 6, lines 58-60 and column 7, lines 7-10) to the contact pads 614 of the wiring substrate 602 via conductor tracks (shown in FIG. 8) of the interconnection film 608/800.

Regarding claim 18, note that, as shown in FIG. 6A and FIG. 6C, the interconnection film 608/800 is arranged on a rear side of semiconductor chip 604.

Regarding claim 20, note that, as shown in FIG. 6A and FIG. 6C, that the base semiconductor component and the stacked semiconductor component (comprising chip 606) are electrically connected via the stack contact areas of the interconnection film 608/800.

Regarding claims 29 and 34, Kim discloses, in FIG. 6A, FIG. 6C, and FIG. 8, a semiconductor component stack having a base semiconductor component comprising: a semiconductor chip 604 arranged centrally (shown in FIG, 6C) on a stiff wiring substrate 602 (called a printed circuit board by Kim), wherein an active upper side of the semiconductor chip 604 (the side with the solder balls 610) faces toward the wiring

substrate 602; the wiring substrate 602 has, in its edge regions, contact pads 614 which are electrically connected to external contacts 616 (not explicitly disclosed by Kim but shown in FIG. 1 and FIG. 2 and thus implied as present in the invention of Kim) and at the same time to contact areas of the semiconductor chip 604 (see column 4, lines 25-29 and column 6, lines 58-62, and note that the electrical contact between the chips will be made through the contact pads 614) and also to stack contact areas (shown in FIG. 8); and the stack contact areas (show in FIG. 8) simultaneously form an upper side of the base semiconductor component (shown in FIG. 6A) and have an arrangement pattern (shown in FIG. 8) corresponding to an arrangement pattern of external contacts of a semiconductor component to be stacked (chip 606).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16, 17, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim.

Regarding claims 16, Kim discloses all of the limitations of claim 15 as described above, and that the semiconductor chip 604 has flip-chip contacts (solder balls 610) which are connected via wiring lines to the contact pads 614 (see column 4, lines 25-29 and column 6, lines 58-62, and note that the electrical contact between the

chips will be made through the contact pads 614), and via through contacts (not explicitly disclosed by Kim but shown in FIG. 1 and FIG. 2 and thus implied as present in the invention of Kim) to the underside of the wiring substrate 602 to external contact areas, the external contact areas having the external contacts 616 (shown in FIG. 6C).

Kim differs from the claimed invention in that Kim does not disclose that the wiring lines are formed on both the upper side and the lower side of the wiring substrate 602.

However, it is commonly known in the art to use circuit boards with wiring lines on both side and therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use wiring on both sides of the wiring substrate 602, to connect the contacts pads 614 on the upper side of the substrate 602 with the contacts 616 on the lower side of the substrate.

One of ordinary skill in the art at the time of the invention would be motivated to do this in order to efficiently route the wiring substrate as is commonly known in the art.

Regarding claim 17, Kim differs from the claimed invention in that Kim does not disclose that the external contacts are arranged in a matrix.

However, it is common in the art to arrange contacts in a matrix, for example FIG. 4, FIG. 5A, FIG. 6B, and FIG. 8 of Kim all show contacts for solder balls arranged in matrices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to also arrange the external contacts in a matrix.

One of ordinary skill in the art would be motivated to do this in order to use a standard and commonly used connection layout.

Regarding claim 25, Kim discloses, in FIG. 6A, FIG. 6C, and FIG. 8, a method for the production of a base semiconductor component comprising: producing a stiff wiring carrier 602 (called a printed circuit board by Kim), with a central semiconductor chip 604 having an active upper side (the side with solder balls 610) disposed (shown in FIG. 6A) on the upper side of the wiring carrier 602, the wiring carrier having contact pads 614 in edge regions of the upper side (shown in FIG. 6A) and external contact areas 616 (called solder balls by Kim, and shown in FIG. 6C) on an underside of the wiring carrier 602, the external contact areas 616 and the contact pads 614 (not explicitly disclosed by Kim but shown in FIG. 1 and FIG. 2 and thus implied as present in the invention of Kim) and also contact areas (see column 4, lines 25-29 and column 6, lines 58-62) of an integrated circuit of the semiconductor chip 604 being electrically connected to one another; producing a deformable interconnection film 608/800 (see FIG. 6A, FIG. 8, and column 6, lines 53-65, and note that TAB tape is deformable)with stack contact areas on its upper side (shown in FIG. 8), which have an arrangement pattern (also shown in FIG. 8) that is congruent with respect to an arrangement pattern of external contacts of a semiconductor component 606 to be stacked, with conductor tracks which are connected to the stack contact areas (shown in FIG. 8) and extend right into the edge regions of the deformable interconnection film 608a/800, the conductor tracks having an arrangement pattern that is congruent with respect to the arrangement pattern of the contact pads (shown in FIG. 8); applying the interconnection film by its underside (shown in FIG. 6a) onto the wiring carrier 602 with semiconductor

chip 604; and deforming (column 7, lines 7-10) the edge sides of the interconnection film 608/800 with the conductor tracks being connected to the contact pads 614.

Kim differs from the claimed invention in that Kim does not disclose whether the conductor tracks are on the underside or the top of the interconnection film 608a/800.

However, as there are only two options for the interconnection film (top or underside) the claim would have been obvious because "a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." *KSR International Co. V. Teleflex Inc.*, 550 U.S. at ___, 82 USPQ2d at 1391

Additionally, one of ordinary skill in the art would be motivated to use a structure where the conductor tracks are on the underside of the interconnection film 608a/800 in order to form the devices as illustrated in FIG. 6C of Kim and avoid having to bend the conductor film in a 180 degree loop in order to contact the traces to the pads 614.

Claims 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Lynch et al. (US 5,681,777) (Lynch hereinafter).

Regarding claim 21, Kim discloses all of the limitations of claim 15 but differs from the claimed invention in that Kim does not disclose that the interconnection film 608/800 has a plurality of mutually insulated layers with conductor tracks.

Lynch discloses, in FIG. 4A, a TAB tape (column 12, lines 54-65) comprising a plurality of mutually insulated layers 410, 440, and 460 with conductor tracks 412, 414, 416.

Therefore, in view of Lynch it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Kim by using a multilayered tape that has a plurality of mutually insulated layers with conductor tracks for the interconnection film 608/800.

One of ordinary skill in the art would be motivated to do this in order to separate the signal lines from the ground and the power lines and thereby create a more electrically advantageous structure.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Buschow et al. ("Encyclopedia of Materials - Science and Technology, Volumes 1-11") (Buschow hereinafter).

Regarding claim 22, Kim discloses all of the limitations of claim 15 but does not disclose that the semiconductor chip 604 of the base semiconductor component is embedded in a plastics composition.

Buschow, in FIG. 1 and the second column on page 8332, discloses the use of plastic underfill (specifically a thermosetting polymeric resin) in order to secure a flip-chip package to a carrier.

Therefore, in view of Buschow, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Kim by using a plastic underfill to secure the semiconductor chip 604 to the wiring substrate 602.

One of ordinary skill in the art would be motivated to do this in order to reduce early package failure do to solder fatigue.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claim 25 above, and further in view of Buschow et al. ("Encyclopedia of Materials - Science and Technology, Volumes 1-11") (Buschow hereinafter).

Regarding claim 27, Kim discloses all of the limitations of claim 25 but does not disclose that before applying the interconnection film 608/800, embedding the semiconductor chip 604 in a plastics composition.

Buschow discloses, in FIG. 1 and the second column on page 8332, the use of plastic underfill (specifically a thermosetting polymeric resin) in order to secure a flip-chip package to a carrier.

Therefore, in view of Buschow, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Kim by using a plastic underfill, prior to applying the interconnection film, to secure the semiconductor chip 604 to the wiring substrate 602.

One of ordinary skill in the art would be motivated to do this in order to reduce early package failure do to solder fatigue and secure the chip 604 in place prior to applying the interconnection film 608/800.

Claims 24 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of Chun (US 6,291,259) (Chun hereinafter).

Regarding claims 24 and 28, Kim discloses all of the limitations of claims 15 and 25 as described above but differs from the claimed invention in that Kim does not disclose that the connection locations between contact pads 614 and conductor tracks of the interconnection film 608/800, in the edge regions of the wiring substrate 602, are embedded in a plastic covering.

Chun, in FIG. 5E and FIG. 5F, discloses using a plastic covering 28 (specifically a molding resin) to encapsulate the ends of conductors 4 after attaching the conductors 4 to contact pads.

Therefore, in view of Chun, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the invention of Kim by embedding the connection locations between contact pads 614 and conductor tracks of the interconnection film 608/800 in a plastic covering after the conductor tracks have been connected to the contact pads.

One of ordinary skill in the art would be motivated to do this in order to protect and more fully secure the connections as is well known in the art.

Allowable Subject Matter

Claims 19 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 30-33 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not disclose or suggest a supporting plate located between a semiconductor chip on a wiring substrate, with the active side of the chip (that is the side of the chip with the connections) facing away from the supporting plate and towards the wiring substrate, and a deformable interconnection film that is deformed in its edges towards the wiring substrate.

Response to Arguments

Applicant's arguments filed 07/14/2009, with respect to the objections to the claims and the rejection under 35 U.S.C. § 112 have been fully considered and are persuasive. The objections to the claims and the rejections under 35 U.S.C. § 112 of the action dated 04/14/2009 have been withdrawn.

Applicant's arguments with respect to claims 15-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Specifically:

1. Papageorge et al. (US 5,438,224) which discloses two IC chips with a deformable interposed substrate between them, but attached in a face-to-face arrangement;

2. Light et al. (US 6,255,723) which discloses, in FIG. 9, a deformable two metal connector;
3. Shim et al. (US 7,309,913) which discloses two IC chips with a deformable interposed substrate and a supporting plate between them, but in a face-to-face arrangement;
4. Baek et al. (US PGPUB 2003/0210533) which discloses a multi-chip package with a flexible intermediate layer that is encapsulated in a plastic covering.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAREN WOLVERTON whose telephone number is (571) 270-5784. The examiner can normally be reached on Monday to Thursday from 9:30 a.m. to 3:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. W./
Examiner, Art Unit 2813

/Matthew C. Landau/
Supervisory Patent Examiner, Art Unit 2813

DW